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December 28, 2001  
Date

Denise Sheridan  
Denise Sheridan

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants : Brian W. Huber and David R. Brown      Attorney Docket No.: 500125.02  
Serial No. : 10/007,871 ✓      Group Art Unit : Not yet assigned  
Filed : November 13, 2001      Examiner : Not yet assigned  
Title : METHOD AND APPARATUS FOR PHASE-SPLITTING A CLOCK SIGNAL

**SUPPLEMENTAL PRELIMINARY AMENDMENT**

Box Non-Fee Amendment  
Commissioner of Patents  
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows:

**In the Title:**

Please replace the title with the following rewritten title:

-- METHOD OF SCALING DIGITAL CIRCUITS AND CONTROLLING THE  
TIMING RELATIONSHIP BETWEEN DIGITAL CIRCUITS --

**In the Specification:**

Please replace the paragraph beginning at page 9, line 23, with the following rewritten paragraph:

-- In the field of semiconductors, it is common to scale up or down the size of components in circuits depending upon the load to be driven by the circuit. Thus, the inverters used in the phase splitters 40, 40', 80, 80', 100, 102. However, as also understood in the art, there is a limit to how small semiconductor components can be scaled. Thus, when the phase splitters 40, 40', 80, 80', 100, 102 are scaled to their minimum size, the relative size of the inverters can change. In particular, the output inverters 48, 54 can continue to be scaled downwardly beyond the point that the input inverters 46, 50 can no longer be scaled down.

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